SYLLABUS: ECE 374 COMPUTER ORGANIZATION

BASIC COURSE INFORMATION

Course prefix, number(s), and title: ECE 374 Computer Organization
Number of credits: 4 (Undergraduate)
Term and year: Spring 2015

Instructor's name: Sudarshan K. Srinivasan
Office location: ECE 101P
Office hours: MWF 2PM-3PM
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BULLETIN DESCRIPTION

Organization and structure of the major sections of a computer: CPU, memory, and I/O system organization and implementation issues. 3 lectures and 1 two-hour VHDL-based laboratory. Prereqs: ECE 275 and ECE 173 with a grade of C or better.

COURSE OBJECTIVES

Upon successful completion of this course, students will understand computer system performance, instruction set architecture, pipelined processor design, memory hierarchy, storage, and I/O. Specifically, students will be able to demonstrate the following:

- Compute and compare performance of Computer Systems
- Encode basic high-level programming language constructs in assembly language.
- Design single-cycle and pipelined microprocessors
- Identify hazards in pipelined microprocessor designs
- Design memory systems
- Implement digital designs in VHDL
- Simulate, test, and debug digital designs

REQUIRED TEXTS

1. David A. Patterson and John L. Hennessy , 4th edition of Computer Organization and Design: The Hardware/Software Interface, Morgan Kaufmann, 2012.
2. S. Brown and Z. Vranesic, 3rd edition of Fundamentals of Digital Logic with VHDL Design, McGraw-Hill, 2009.

COURSE SCHEDULE/OUTLINE/CALENDAR OF EVENTS

Week	Topic	Reading /Assignment
1	Introductions; Performance	H&P Chapter 1, Sections 1.1-1.4
2	Power and multiprocessor systems	H&P Chapter 1, Sections 1.5-16
3	Arithmetic and memory operations	H&P Chapter 2, Sections 2.1-2.5
4	Logical operations	H&P Chapter 2, Section 2.6
5	**Test 1**; Instructions for making decisions	H&P Chapter 2, Section 2.7
6	Implementing sequential elements in VHDL	B&V Chapter 7
7	ISA design	H&P Chapter 4, Sections 4.1-4.4
8	Pipelined design	H&P Chapter 4, Sections 4.5-4.6
9	Pipeline hazards	H&P Chapter 4, Sections 4.7-4.9
10	**Test 2**; Basics of Cache	H&P Chapter 5, Section 5.2
11	Cache cont.	H&P Chapter 5, Section 5.3
12	Virtual memory	H&P Chapter 5, Section 5.4
13	Basics of Storage	H&P Chapter 6, Sections 6.1-6.2
14	Disk and flash storage	H&P Chapter 6, Sections 6.3-6.4
15	I/O	H&P Chapter 6, Sections 6.5-6.6
16	Multicores and Multiprocessors	H&P Chapter 7, Sections 7.1-7.2
17	**Final Exam**	

- *Instructor reserves the right to modify course schedule.*

EVALUATION PROCEDURES AND GRADING CRITERIA

The course includes 10 lab assignments, 10 homework assignments, 2 tests, and one final exam. Laboratory assignments will include implementation and simulation of microprocessor logic components in VHDL. Lab assignments should be completed in groups of two. The weighted assignment of each of the course components are given below. Each lab assignment is worth 2.5% of the final grade. Each homework assignment is worth 2% of the final grade.

Weighted Assignments (%):

1. 10 Laboratory Assignments: 25% of final grade
2. 10 Homework Assignments: 20% of final grade
3. Test 1: 15% of final grade
4. Test 2: 15% of final grade
5. Final Exam: 25% of final grade

Final Course Grade Scale:

1. A = 90% to 100%
2. B = 80% to 89.90%
3. C = 70% to 79.90%
4. D = 60% to 69.90%
5. F = 0% to 59.90%

CLASS ATTENDANCE POLICY:

Class attendance is not required. However, the student is responsible to obtain information about any course-related announcements made in class. These announcements may not be repeated and may not be communicated via other means.

MISSED AND LATE ASSIGNMENTS/EXAMS POLICY:

No late assignments will be accepted unless for medical reasons and emergencies. It is recognized that sometimes an assignment is impossible to make-up. The student must inform and obtain permission from the instructor prior to the date of a test/exam, to be given the opportunity for a make-up exam. For excuses related to medical and emergency situations, the student must provide supporting documentation.

AMERICAN DISABILITIES ACT FOR STUDENTS WITH SPECIAL NEEDS STATEMENT

"Any students with disabilities or other special needs, who need special accommodations in this course are invited to share these concerns or requests with the instructor and contact the Disability Services Office as soon as possible."

STUDENT VETERANS AND SOLDIERS STATEMENT

"Veterans and student soldiers with special circumstances or who are activated are encouraged to notify the instructor in advance."

ACADEMIC HONESTY STATEMENT

"*The academic community is operated on the basis of honesty, integrity, and fair play. NDSU Policy 335: Code of Academic Responsibility and Conduct applies to cases in which cheating, plagiarism, or other academic misconduct have occurred in an instructional context. Students found guilty of academic misconduct are subject to penalties, up to and possibly including suspension and/or expulsion. Student academic misconduct records are maintained by the Office of Registration and Records. Informational resources about academic honesty for students and instructional staff members can be found at www.ndsu.edu/academichonesty*."

College of Engineering Honor Code statement:

"Each student is required to sign the College of Engineering Honor Code. As outlined in the Honor Code, all students are required to have a signed 'Honor Pledge' form in their CoE advising file. Students are only required to sign the form once. Link to additional information: http://www.ndsu.edu/cea/undergraduate_students/honor_code/"