For the following exam, **answer 8 out of the following 10 questions**. Each question is worth 12.5 points. **Circle the 8 questions below, Q1-Q10, that you want graded**:

Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10

1) The values of the function F(A, B, C, D) are given by the following truth table. Find the minimum sum-of-products (SOP) and product-of-sums (POS) Boolean representations of F, named F_{SOP} and F_{POS}, respectively.

A	B	C	D	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

2) You have only one 7402 IC chip (quad 2-input NOR) available to implement G = (A+B)•C'•D'. Show the corresponding logic diagram.

3) $A = 10010110_2$ $B = 1111010_2$

a) If *A* and *B* are **unsigned** numbers, what is A × B in binary? Show the partial products.

b) If *A* and *B* are **2^s complement** numbers, what is A + B? Show your work.

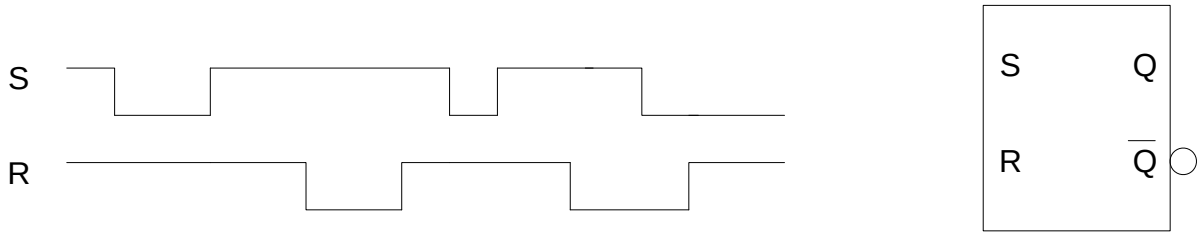
c) If *A* and *B* are **unsigned** numbers, what is A – B using 2^s complement subtraction? Show your work.

4) a) Convert $+243.647_{10}$ into a **2^s complement** binary number, showing 10 digits in the integer portion and five digits in the fractional portion. Show your work.

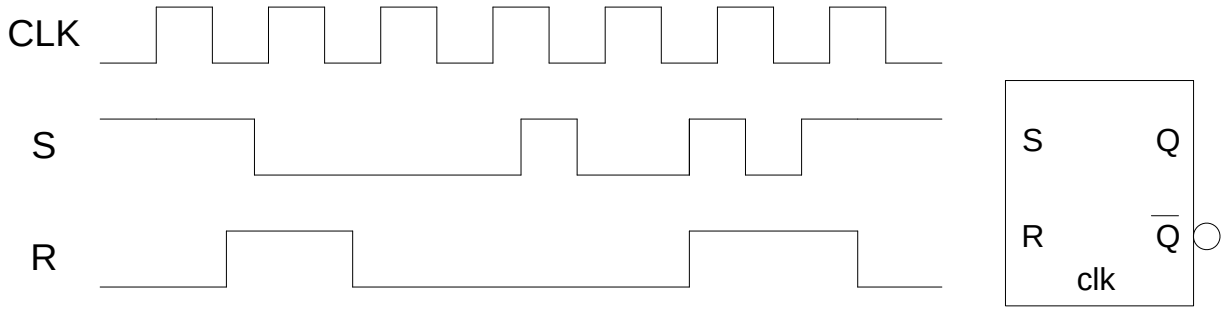
b) $8A6.48_{16}$ is a **sign magnitude** number. Convert it into a decimal number. Show your work.

5) Program the following MUX to implement the function:
G = (A+B'+C)(A+C'+D')(B'+C+D')(B+C+D). Do not use any additional logic gates.

6a) Draw the output waveforms, Q and Q', for an active-high SR latch. Initially, Q = 0 and Q' = 1.



b) Show the output waveforms, Q and Q', for an active high clocked SR latch. Initially, Q = 0 and Q' = 1.



7) Design a maximum speed, minimal area **CMOS** implementation of a BCD (Binary Coded Decimal) detector, which asserts output, *F*, when input, *X(3:0),* is not a valid BCD number.

8) Design a positive edge-triggered LM flip-flop using only combinational logic and a basic positive edge-triggered D flip-flop (i.e., *D* and *clk* inputs only). The LM flip-flop operates as follows: when L=0 the output is loaded with the complement of *M* (i.e., M'); when L=1 and M=0 the output is toggled; and when L=1 and M=1 the output is reset to 0. The resulting design should be optimized for the minimal number of gates and minimal delay.

9) Draw the circuit diagram for a 4-bit **2^s complement** counter that operates as follows: if control = 1 then $count^+ = count^- + 1_{10}$; else $count^+ = count^- - 2_{10}$. An additional output, *OV*, is asserted iff the correct value of $count^+$ cannot be represented in 4 bits. Use FAs, HAs, and additional logic as necessary, and DFF0 components (i.e., DFFs with a reset-to-0 input) such that the count is resettable to zero.

10) For the following state machine, derive the next state and output equations **in minimal SOP form**. The state variables are *Qa*, *Qb*; the input is *X*; the Moore output is *Y*; and the Mealy output is *Z*. Show your work.